type OW smd clock oscillator (5.0 x 3.2)mm Feb 7th 2014

Type OW smd clock oscillator (80 ~ 320)MHz, output PECL or LVDS (5.0 x 3.2)mm, height 1.30mm low jitter

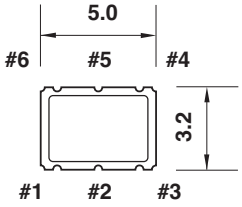
A very high frequency, smd clock oscillator manufactured over the frequency range of 80MHz ~ 320MHz.

Low jitter, 3rd overtone crystal design, +3.3V d.c. and 2.5Vd.c. supply.

An industry standard ceramic (5.0 x 3.2)mm package providing an excellent combination of parameters within a small smd enclosure.

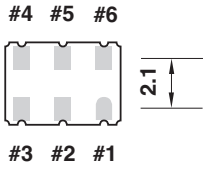
Supplied on tape and reel with 1000 and 3000 pieces per reel.

Dimensions(mm)

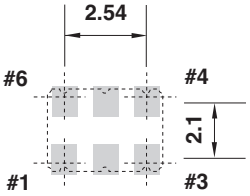


top view

pad connections:
#1 tri-state/ NC
#2 NC/ tri-state
#3 ground
#4 output
#5 complimentary output
#6 V_{DD}



pads viewed from bottom pad size (0.9 x 0.64)mm



suggested land pattern pad size (1.2 x 0.85)mm

connect 0.1µF capacitor between V_{DD} and ground - pads #6 and #3

Frequency stability -vs- temperature:

TEMP. RANGE	COMBINED TOLERANCE		
(-10 +60)°C	±25ppm	±50ppm	±100ppm
(-20 +70)°C	±25ppm	±50ppm	±100ppm
(-40 +85)°C		±50ppm	±100ppm

Tolerance inclusive of calibration tolerance at +25°C, temperature tolerance, load variation and supply voltage variation, first year ageing, vibration and shock

Electrical specification:

	PECL				LVDS				
	3.3Vd.c.		2.5Vd.c.		3.3Vd.c.		2.5Vd.c.		
	min.	max.	min.	max.	min.	max.	min	max.	
supply voltage V_{DD} ±5%	3.135	3.465	2.375	2.625	3.135	3.465	2.375	2.625	Vd.c.
frequency range	(80 ~ 320)MHz								MHz
standard frequencies	106.25, 125, 155.52, 156.25, 187.5, 212.5, 312.5								MHz
supply current (80 ~ 160)MHz	-	75	-	75	-	50	-	50	mA
supply current (160 ~ 250)MHz	-	100	-	100	-	50	-	50	mA
supply current (250 ~ 320)MHz	-	100	-	100	-	65	-	65	mA
o/p high (logic 1)	2.275	-	1.475	-	-	1.6	-	1.6	V
o/p low (logic 0)	-	1.68	-	1.095	0.9	-	0.9	-	V
rise and fall time, t_r	-	1.0	-	1.0	-	1.0	-	1.0	nano sec.
start up time	-	3	-	3	-	3	-	3	milli sec.
tri-state to pin #1 or #2: active o/p	$0.7V_{DD}$	-	$0.7V_{DD}$	-	$0.7V_{DD}$	-	$0.7V_{DD}$	-	V
tri-state to pin #1 or #2: high impedance o/p	-	$0.3V_{DD}$	-	$0.3V_{DD}$	-	$0.3V_{DD}$	-	$0.3V_{DD}$	V
RMS phase jitter(integrated 12kHz ~ 20MHz)									
80MHz < f_0 <125MHz	-	0.9	-	0.9	-	0.9	-	0.9	pico.sec
125MHz < f_0 <150MHz	-	0.7	-	0.7	-	0.7	-	0.7	
150MHz < f_0 < 200MHz	-	0.5	-	0.5	-	0.5	-	0.5	
f_0 > 200MHz	-	0.3	-	0.3	-	0.3	-	0.3	
phase noise +100 Hz	-	-70	-	-70	-	-70	-	-70	dBc/Hz
phase noise +1 kHz	-	-100	-	-100	-	-100	-	-100	
phase noise +10 kHz	-	-125	-	-125	-	-125	-	-125	
ageing	-	±3	-	±3	-	±3	-	±3	ppm
storage temperature range	(-55 +125)°C								°C

Telephone: +44 (0)1903 740000, e-mail: sales@tfc.co.uk

Ordering information

EXAMPLE	type OW smd clock oscillator, 155.52MHz, +3.3Vd.c. supply, inhibit on pin #2, ±50ppm(-10 +60)°C, output PECL
TFC PART NUMBER	**OW 155.52M E T G I L**
OW	type: OW = clock oscillator type OW, smd, (5.0 x 3.2)mm
155.52	frequency: 155.52MHz, frequency range (80 ~ 320)MHz
E	supply voltage: E = +3.3Vd.c.
T	inhibit pin: T = inhibit on pin #2(standard configaration)
G	frequency stability: G = ±50ppm
I	temperature range: I = (-10 +60)°C
L	output: L = PECL
OPTIONS	
supply voltage	E: +3.3Vd.c., J: +2.5Vd.c.
inhibit pin	T: inhibit on pin #2(standard), R: inhibit on pin #1(case by case option)
frequency stability	D: ±25ppm, G: ±50ppm, H: ±100ppm
temperature range	I: (-10 +60)°C, C: (-20 +70)°C, L: (-40 +85)°C
output	L: PECL, V: LVDS

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