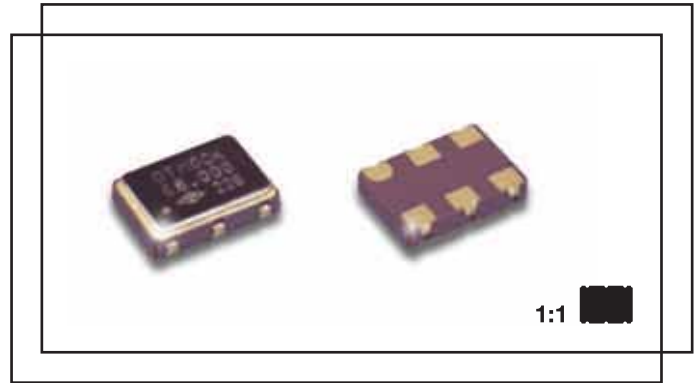


Type OT multiplier clock osc (100 ~ 700)MHz

- # tight symmetry
- # (7.0 x 5.0)mm footprint
- # +3.3Vd.c. supply
- # RoHS compliant



Electrical specification

Case style	T: (7.0 x 5.0)mm, height 1.80mm	
Frequency range	(100 ~ 700)MHz	
Stability *	±(25 ~ 100)ppm, temperature range dependent	
Supply voltage V_{dd}	+3.3Vd.c. ±10%	
Supply current max.	(100 ~ 160)MHz	75mA max. PECL 65mA max. LVDS
	(160 ~ 700)MHz	100mA max. PECL 80mA max. LVDS
Rise and fall time max. **	1ns max.	
Start up time	3milli sec.	
Operating temperature	(-10 +60)°C ~ (-40 +85)°C	
Storage temperature	(-55 +125)°C	
Output	PECL, LVDS	
Phase jitter, integrated 12kHz ~ 20MHz	4ps max.	
Symmetry	(45 ~ 55)%	
Ageing	±5ppm first year max.	

* inclusive of calibration tolerance at +25°C, temperature tolerance, supply voltage variation, load variation, first year ageing, shock and vibration.

** measured between (20 ~ 80)% V_{dd}

Ordering information

Example type OT multiplier smd clock oscillator, 320MHz, +3.3Vd.c., ±50ppm(-20 +70)°C, output PECL, symmetry (45 ~ 55)%

TFC PART NUMBER OTM 320M E G C L

'OTM' type number: OTM = smd clock oscillator type OT multiplier
 '320M' frequency: 320M = 320MHz, frequency range from (100 ~ 700)MHz
 'E' supply voltage: E = +3.3Vd.c.
 'G' frequency stability: G = ±50ppm
 'C' temperature range: C = (-20 +70)°C
 'L' output logic and symmetry: L = PECL (45 ~ 55)%

Supply voltage: E = +3.3Vd.c.

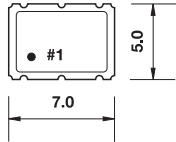
Frequency stability: D = ±25ppm, G = ±50ppm, H = ±100ppm

Temperature range: I = (-10 +60)°C, C = (-20 +70)°C, L = (-40 +85)°C

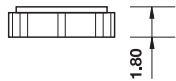
Output logic and symmetry: L = PECL (45 ~ 55)%, V = LVDS (45 ~ 55)%

Type OT multiplier clock oscillator

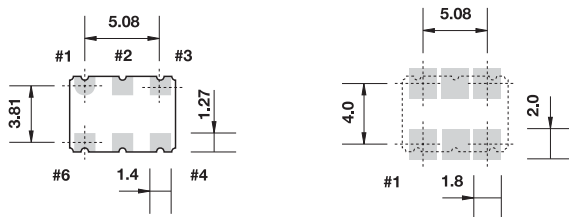
OT multiplier dimensions(mm) shown twice full size



Suggested land pattern



Connect 0.1µF capacitor between Vdd and ground



Pads viewed from bottom

- #1 N/C
- #2 tri-state
- #3 ground
- #4 output
- #5 complimentary output
- #6 Vdd

Output inhibit: pad #2:

- +2.5Vd.c. min, 3.3Vd.c. supply: output active
- +0.5Vd.c. max: output high impedance