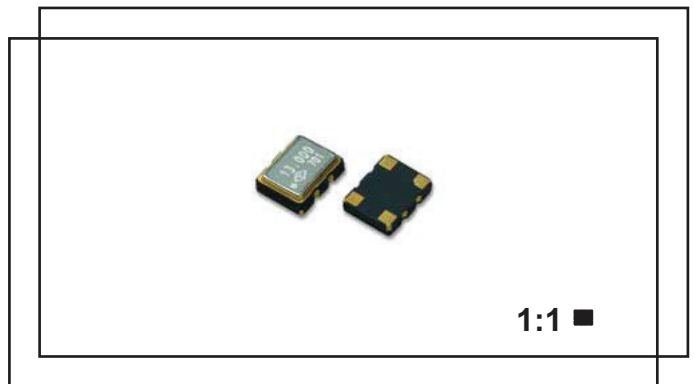


Type PY smd clock oscillator smd ceramic package (1.00 ~ 200)MHz

- # tight symmetry, low jitter
- # (2.5 x 2.0)mm footprint
- # +(1.8, 2.5, 3.3)Vd.c. supply
- # RoHS compliant



Electrical specification

Case style Y: (2.5 x 2.0)mm, height 1.0mm max.
 Frequency range (1.00 ~ 133)MHz: 1.8V, (1.00 ~ 166)MHz: 2.5V, (1.00 ~ 200)MHz: 3.3V
 Stability * $\pm(20 \sim 100)$ ppm, temperature range dependent

Supply voltage $V_{DD} \pm 10\%$		+1.8Vd.c.	+2.5Vd.c.	+3.3Vd.c.
Supply current max.	$1\text{MHz} \leq F_0 < 30\text{MHz}$	6mA	8mA	10mA
	$30\text{MHz} \leq F_0 < 75\text{MHz}$	8mA	10mA	15mA
	$75\text{MHz} \leq F_0 < 133\text{MHz}$	12mA	15mA	20mA
	$133\text{MHz} \leq F_0 < 166\text{MHz}$	-	15mA	22mA
	$166\text{MHz} \leq F_0 < 200\text{MHz}$	-	-	25mA

Standby current max.		15 μ A		
Start time max.		5mSec.		
Absolute clock period jitter (frequency dependent)		(40 ~ 200)pSec		
Rise and fall time max. **	$1\text{MHz} \leq F_0 < 10\text{MHz}$	5nSec	4nSec	3nSec
	$10\text{MHz} \leq F_0$	4nSec	3nSec	2nSec

Operating temperature (-10 +60) $^{\circ}$ C ~ (-40 +85) $^{\circ}$ C
 Storage temperature (-55 +125) $^{\circ}$ C
 Output CMOS, 15pF
 Symmetry (45 ~ 55)%, (40 ~ 60)%
 Tri-state (input to pin 1) - Output active / High impedance 0.7 V_{DD} min. / 0.3 V_{DD} max.

* inclusive of calibration tolerance at +25 $^{\circ}$ C, temperature tolerance, supply voltage variation, load variation, first year ageing(10 years for types S and J), shock and vibration.
 ** measured, with an output load of 15pF, between (10 ~ 90)% V_{DD}

Ordering information

Example type PY oscillator, 13.00MHz, +3.3Vd.c., tri-state, ± 25 ppm(-20 +70) $^{\circ}$ C, CMOS 15pF, (45 ~ 55)%

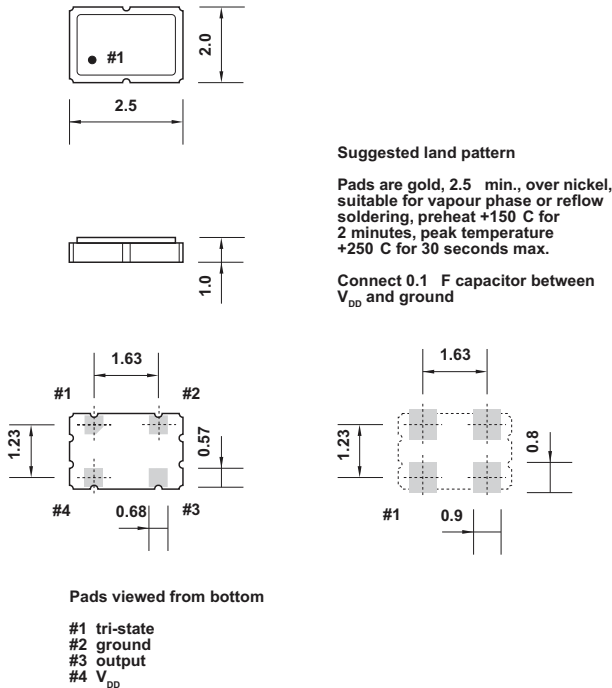
TFC PART NUMBER PY 13.00M E T D C J

'PY' type number: PY = smd clock oscillator type PY
 '13.0M' frequency: 13.0M = 13.00MHz, frequency range from (1.0 ~ 200)MHz
 'E' supply voltage: E = +3.3Vd.c., J = +2.5Vd.c., K = +1.8Vd.c.
 'T' tri state: T = tri-state with programmed frequency, tri-state function on pin #1
 'D' frequency stability: D = ± 25 ppm
 'C' temperature range: C = (-20 +70) $^{\circ}$ C
 'J' output logic and symmetry: J = CMOS 15pF, (45 ~ 55)%

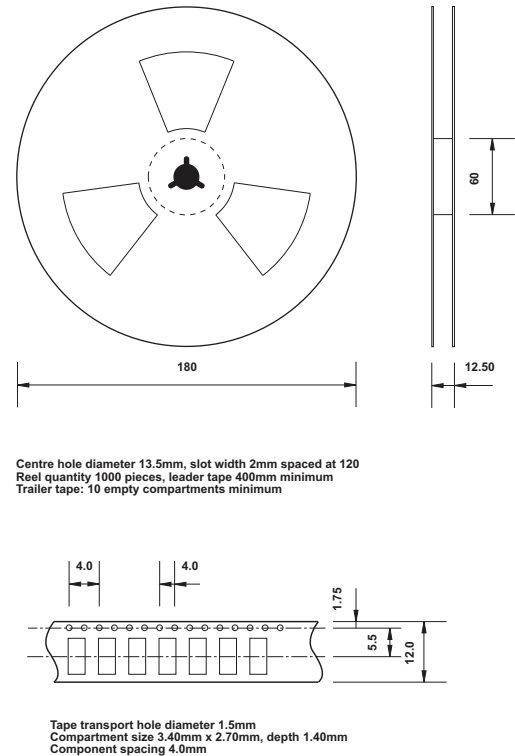
Frequency stability C: ± 20 ppm, D: ± 25 ppm, G: ± 50 ppm, H: ± 100 ppm
 Temperature range I: (-10+60) $^{\circ}$ C, C: (-20 +70) $^{\circ}$ C, D: (-30 +80) $^{\circ}$ C, L: (-40 +85) $^{\circ}$ C
 Output J: CMOS 15pF(45 ~ 55)%, F: CMOS 50pF(45 ~ 55)%
 K: CMOS 15pF(40 ~ 60)%, G: CMOS 50pF(40 ~ 60)%

Type PY clock oscillator

PY dimensions(mm) shown twice full size



Tape and reel dimensions(mm)



Environmental test conditions (on request)

Mechanical shock	1500g, half sine wave, 0.5ms, 3 directions	MIL STD 883D 2002.3, condition A
Thermal shock	(-55 ~ +125)°C, 20 cycles	MIL STD 883D 1011.9, condition B
Vibration	(10 ~ 2000)Hz, 1.25mm, sine wave, 20g, each of three planes, duration 4 hours	MIL STD 883D 2005.2, condition B
Solderability	+245°C ±5°C, 5 seconds ±0.5 seconds	MIL STD 883D 2003.7
Fine leak	Mass spectrometer leak rate less than 2 ¹⁰⁻⁸ atm.cc/sec. helium	MIL STD 883D 1014.9, condition A
Gross leak	Leak test in de-ionised water, vacuum 70cm/Hg	
Humidity	85% relative humidity, +85°C, 500 hours	JIS-C 7022 B-5, condition C