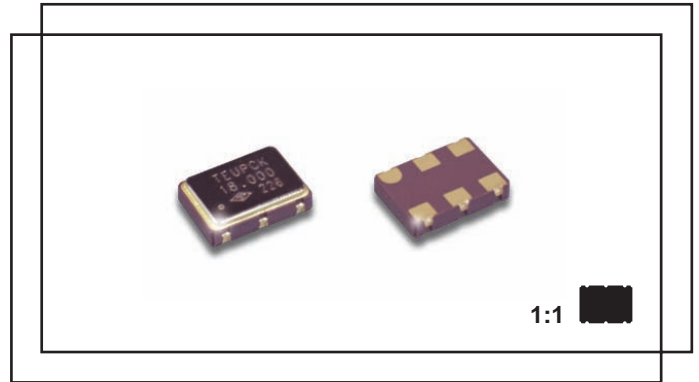


Type VT
smd ceramic package
(1.5 ~ 200.0)MHz

- # **tight symmetry**
- # **(7.0 x 5.0)mm footprint**
- # **+3.3Vd.c., +5.0Vd.c. supply**



Electrical specification

Case style T: (7.0 x 5.0)mm, height 2.0mm (max.)
Frequency range (1.5 ~ 80)MHz (5.0V supply) or (1.5 ~ 200.0)MHz (3.3V supply)
Stability * $\pm(25 \sim 50)$ ppm, temperature range dependent
Pulling range ± 100 ppm min.
Control voltage V_t (+2.5 \pm 2.0)Vd.c., $V_{cc} = +5.0$ Vd.c., (+1.65 \pm 1.35)Vd.c., $V_{cc} = +3.3$ Vd.c.

Supply voltage $V_{cc} \pm 10\%$		+3.3Vd.c.	+5.0Vd.c.
Supply current max.	(1.5 ~ <20.0)MHz	10mA	15mA
	(20.0 ~ <50.0)MHz	20mA	30mA
	(50.0 ~ <80.0)MHz	30mA	35mA
	(80.0 ~ <160.0)MHz	40mA	-
	(160.0 ~ 200.0)MHz	50mA	-
Rise and fall time max. **	(1.5 ~ <20.0)MHz	10nS	8nS
	(20.0 ~ <50.0)MHz	6nS	5nS
	(50.0 ~ <80.0)MHz	5nS	5nS
	(80.0 ~ <200.0)MHz	5nS	-
Tri-state (input to pin 2 or pin 5)	output active	2.0V min.	4.0V min.
	output in high impedance	0.5V max.	0.8V max.
Output level (CMOS)	output high (logic 1)	-	90% V_{cc}
	output high (logic 0)	10% V_{cc}	-

Linearity 10% max.
Start-up time 10m sec. max.
Operating temperature (-10 +60) $^{\circ}$ C ~ (-40 +85) $^{\circ}$ C
Storage temperature (-55 +125) $^{\circ}$ C
Output CMOS 15pF, CMOS 50pF
Symmetry (45 ~ 55)%
Ageing ± 5 ppm first year max.

* inclusive of calibration tolerance at +25 $^{\circ}$ C, temperature tolerance, supply voltage variation, load variation, first year ageing, shock and vibration.
 ** measured, with an output load of 15pF, between (10 ~ 90)% V_{cc}

Type VT

Ordering information

Example type VT smd clock oscillator, 40.00MHz, ± 100 ppm pulling range, +3.3Vd.c., tri-state to pin 2, ± 25 ppm(-20 +70) $^{\circ}$ C, output CMOS 15pF, symmetry (45 ~ 55)%

TFC PART NUMBER VT 40.0M E U M C J

'VT' type number: VT = smd clock oscillator type VT

'40.0M' frequency: 40.0M = 40.00MHz, frequency range from (1.5 ~ 52.0)MHz

'E' supply voltage: E = +3.3Vd.c., C = +5.0Vd.c.

'U' tri-state function: U = input to pin 2; R = input to pin 5

'M' frequency stability: M = ± 25 ppm

'C' temperature range: C = (-20 +70) $^{\circ}$ C

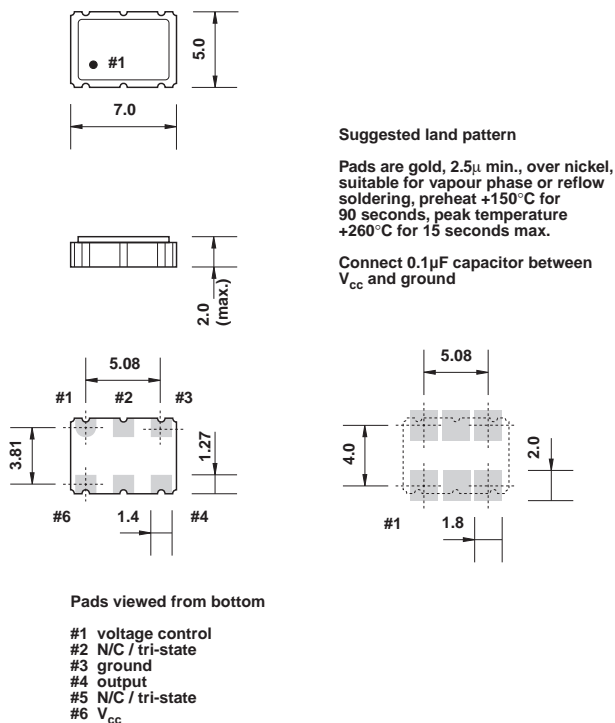
'J' output logic and symmetry: J = CMOS 15pF, (45 ~ 55)%

Frequency stability M: ± 25 ppm, P: ± 50 ppm,

Temperature range C: (-20 +70) $^{\circ}$ C, L: (-40 +85) $^{\circ}$ C

Output J: CMOS 15pF(45 ~ 55)%, F: CMOS 50pF(45 ~ 55)%,

VT dimensions(mm) shown twice full size



Tape and reel dimensions(mm)

