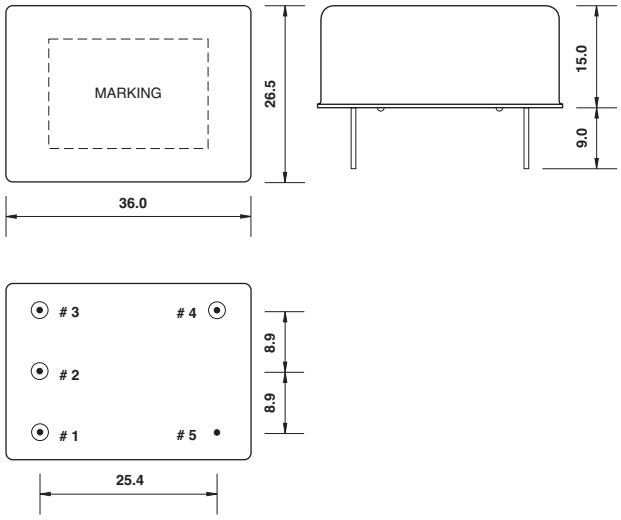
PLL PL936 - 15

- **1MHz to 2.4GHz phase locked loop hybrid TCXO module phase locked to external precision reference.**
- **ECL, sine wave output, sub 1ps jitter.**
- **Hermetically sealed case, 15mm height.**
- **h.f communications equipment, system synchronisation.**

Generic specification:

frequency range:	1MHz ~ 2.4GHz
stability:	
TCXO holdover	from ±1ppm, custom specified
locked	dependent upon input reference accuracy
input reference	10.000MHz, 0dBm, as standard
against V_{cc} change	±0.05ppm max., V_{cc} ±5%
against load change	±0.02ppm max., load ±10%
ageing short term	±0.005ppm max./day
ageing long term	from ±5ppm max., 10 years
output:	single ended PECL, sine wave, CMOS
lock time	30secs max., frequency dependent
supply voltage:	+3.3Vd.c., +5Vd.c., +12Vd.c., ±5%
supply current:	50mA typical, frequency dependent
insulation resistance:	500MΩ min., 100Vd.c.
typical phase noise:	
single sideband, 1Hz bandwidth	-100dBc/Hz, f_o +10Hz -115dBc/Hz, f_o +100Hz -125dBc/Hz, f_o +1kHz
jitter:	1ps max., typical
temperature:	
operating range	customer specified
storage range	(-40 +125)°C
marking:	part number, frequency, date code, serial number

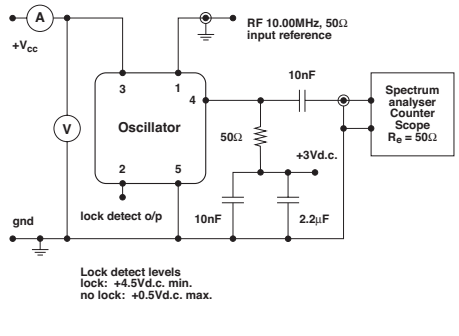
Dimensions(mm):



Pin connections:

#1	RF input reference frequency
#2	lock detect output
#3	supply voltage, V_{cc}
#4	RF output
#5	ground/case

Test circuit:



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